IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Yuri Mirgorodski et al.

Application No.: 10/664,469

Filed: September 17, 2003

For: A METHOD OF PMOS STACKED-GATE MEMORY CELL PROGRAMMING ENHANCEMENT UTILIZING STAIR-LIKE PULSES OF CONTROL GATE VOLTAGE

Confirmation No.: Unknown

Group Art Unit: Unknown

Examiner: Unknown

SUBMISSION OF FORMAL DRAWINGS

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 10, 2003.

STALLMAN & POLLOCK LLP

Dated: 12/10/03 By: _____
Janet Chan

Commissioner for Patents
Attn: Official Draftsperson
P.O. Box 1450
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Sir:

Enclosed are two (2) sheets of formal drawings for filing in the above-referenced application.

Respectfully submitted,

STALLMAN & POLLOCK LLP

Dated: December 10, 2003 By: _____
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Atty Docket No.: NSC1-M3500